What is claimed is:

1. A semiconductor memory device comprising: a plurality of memory cell transistors arranged in a matrix form; a plurality of bit lines and a plurality of word lines to which drains and gates of said memory cell transistors are respectively connected; and a high-potential source line and a low-potential source line to which sources of said memory cell transistors are selectively connected, wherein

the source of each of the memory cell transistors is connected by mask programming to either said high-potential source line or said low-potential source line, depending on data to be held for said each memory cell transistor.

2. A semiconductor memory device as set forth in claim 1, wherein a plurality of said high-potential source lines and a plurality of said low-potential source lines are formed parallel to said plurality of bit lines.

3. A semiconductor memory device as set forth in claim 1, wherein said high-potential source line and said low-potential source line are respectively formed in different wiring layers.

4. A semiconductor memory device as set forth in claim 2, wherein said high-potential source lines and said low-potential source lines are respectively formed in different wiring layers.

5. A semiconductor memory device as set forth in claim 1, further comprising: a decoder for selecting one bit line from among said plurality of bit lines; and a level shifter for supplying a potential intermediate between a high potential and a low potential to said bit line selected by said decoder.